REMARKS/ARGUMENTS

Claims 1, 3, 4, 6-8, and 10-14 are pending in the present application. Claims 1, 4, 8, and 10 have been amended. Claims 1, 4, 8, and 10 are independent claims. The Examiner is respectfully requested to reconsider his rejections in view of the Amendments and the following Remarks.

Rejection Under 35 U.S.C. § 103

Claims 1, 3, 4, 6-8, and 10-14 stand rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,585,817 to Itoh et al. (hereinafter Itoh) in view of U.S. Patent No. 6,127,998 to Ichikawa et al. (hereinafter Ichikawa), U.S. Patent No. 5,355,165 to Kosonocky et al. (hereinafter Kosonocky), and U.S. Patent No. 6,400,404 to Hirota et al. (hereinafter Hirota). This rejection is respectfully traversed.

Independent claims 1, 4, and 8 recite an imaging section including vertical transfer paths, each of which "transfer[s] the signal charges toward one end in accordance with vertical driving pulses."

However, independent claim 1 recites that a display section includes input circuits for "receiving the first signals from said imaging section and outputting second image signals corresponding to the first signals to the image signal input

terminals [of the display section] in parallel column by column." Thus, according to claim 1, the display section's input circuits are configured to transfer signals in parallel column by column. Independent claims 4 and 10 similarly recite that the input circuits of the display section transfer signals "in parallel column by column" to the image signal input terminals of the display section.

In page 4 of the outstanding Office Action, the Examiner asserts that "Itoh does not teach vertical transfer paths such that signals are transferred in parallel column by column." The Examiner further asserts that Kosonocky provides such a teaching, citing col. 6, lines 20-34.

Applicant respectfully submits that the Examiner's assertion mischaracterizes the claimed invention. As discussed above, claims 1, 4, and 10 recite that the **input circuits of the display section** transfer signals in parallel column by column, rather than the vertical transfer paths.

Kosonocky fails to disclose such a feature. In the passage cited by the Examiner, Kosonocky discusses the operation of an **image sensor**. Specifically, in col. 6, lines 20-34, Kosonocky teaches that, with respect to a column of photosensors P_{ij},

> "photo information is sampled from each Pij by means of a clock f1 and transferred to its corresponding register (Gij),"

and, ultimately,

> "the photo information is read out of the registers and transferred in parallel from stage-to-stage along each column by means of a clock f2 and then transferred to a **serial output register.**" (emphasis added)

Here, Kosonocky merely discloses a serial-to-parallel converter connected between each photosensor P_{ij} and a serial output register of the image sensor. As each photosensor P_{ij} samples the N frames of photo information, the frames are transferred serially among storage elements S_{in} in a corresponding storage register G_{ij}. When the elements in the photosensor's storage register G_{ij} are filled, Kosonocky discloses that the N frames are transferred in parallel to the **serial output register** O_{sj}.

Thus, even though Kosonocky teaches that N frames are vertically transferred from each photosensor P_{ij} in parallel, the frames are **output from the image sensor serially**. Accordingly, there is no teaching or suggestion in Kosonocky that any element

receiving the output of the image sensor would receive or transfer the output signals **in parallel column by column.**

Thus, Kosonocky does not teach or suggest input circuits in a display section for receiving image signals and outputting a corresponding set of signals in parallel column by column, as required by independent claims 1, 4, and 10. Furthermore, Applicants submit that none of the other cited references teach or suggest this feature, and that the Examiner does not assert that any of the other cited references teach or suggest this feature.

Furthermore, independent claims 1, 4, and 8 recite that an imaging section includes output circuits "for converting the signal charges arrived at one end of said vertical transfer paths to the first signals and outputting the first signals in parallel column by column of said matrix." Independent claim 10 similarly recites that signals representing an image are output in parallel column by column.

It is clear that the Examiner relies on Hirota to disclose this feature (see Office action at page 4, 3rd full paragraph). The Examiner specifically cites col. 2, lines 3-11 of Hirota. Applicant respectfully disagrees.

Hirota discloses that an imaging device 14 having a matrix of sensors 11 in matrix form. Hirota further discloses vertical

CCDs 13 that sequentially transfer signal charges from the sensors to a horizontal CCD 15. According to Hirota, the horizontal CCD horizontally transfers the signal charges out of the imaging device one line (row) at a time. See Fig. 2 and col. 4, line 31 - col. 5, line 16.

Thus, Hirota clearly discloses that a horizontal transfer path is used for outputting the signals representing an image, one row at a time. Accordingly, Hirota provides no teaching or suggestion of outputting signals representing images in parallel column by column, as required by independent claims 1, 4, 8, and 10. Furthermore, Applicant submits that none of the other cited references teach or suggest this feature, and that the Examiner does not assert that any of the other references provides such a teaching or suggestion.

At least for the reasons set forth above, Applicant respectfully submits that independent claims 1, 4, 8, and 10 are allowable. Furthermore, it is respectfully submitted that claims 3, 6, 7, and 11-14 are allowable at least by virtue of their dependency on claims 1, 3, 8, and 10. Thus, reconsideration and withdrawal of this rejection is respectfully requested.

Conclusion

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but to merely show the state of the art, no comment need be made with respect thereto.

In view of the above Remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. Thus, the Examiner is respectfully requested to reconsider the outstanding rejections and issue a Notice of Allowance in the present application.

Should the Examiner believe that any outstanding matters remain in the present application, the Examiner is respectfully requested to contact Jason W. Rhodes (Reg. No. 47,305) at the telephone number of the undersigned to discuss the present application in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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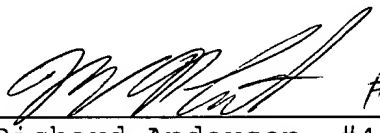
By  #39,491
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